Fast Packet Switching for Integrated Services

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Abstract

As the communications industry continues to expand two current trends are becoming apparent: the desire to support an increasing diversity of communications services (voice, video, image, text, etc.) and the consequent requirement for increased network capacity to handle the expected growth in such multi-service traffic. This dissertation describes the design, performance and implementation of a high capacity switch which uses fast packet switching to offer the integrated support of multi-service traffic. Applications for this switch are considered within the public network, in the emerging metropolitan area network and within local area networks.

The Cambridge Fast Packet Switch is based upon a non-buffered, multi-path switch fabric with packet buffers situated at the input ports of the switch. This results in a very simple implementation suitable for construction in current gate array technology. A simulation study of the throughput at saturation of the switch is first presented to select the most appropriate switch parameters. Then follows an investigation of the switch performance for multi-service traffic. It is shown, for example, that for an implementation in current CMOS technology, operating at 50 MHz, switches with a total traffic capacity of up to 150 Gbits/sec may be constructed. Furthermore, if the high priority traffic load is limited on each input port to a maximum of 80% of switch port saturation, then a maximum delay across the switch of the order of 100 μsecs may be guaranteed, for 99% of the high priority traffic, regardless of the lower priority traffic load.

An investigation of the implementation of the switch by the construction of the two fundamental components of the design in 3 μm HCMOS gate arrays is presented and close agreement is demonstrated between the performance of the hardware implementation and the simulation model. It is concluded that the most likely area of application of this design is as a high capacity multi-service local area network or in the interconnection of such networks.

Preface

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Except where otherwise stated in the text, this dissertation is the result of my own work and is not the outcome of any work done in collaboration. Furthermore, this dissertation is not substantially the same as any that I have submitted for a degree, diploma or any other qualification at any other university. No part of this dissertation has already been or is being concurrently submitted for any such degree, diploma or any other qualification.

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Glossary of Terms

ATD: Asynchronous Time Division, (see page 5).

ATM: Asynchronous Transfer Mode, (see page 5).

BiCMOS: A high speed implementation technology integrating both bipolar and CMOS devices on the same integrated circuit, (see page 110 and table 8.2).

B-ISDN: Broadband ISDN, (see page 5).

CAD: Computer Aided Design.

CAM: Computer Aided Manufacture.

CATV: Community Antenna Television, i.e. cable TV.

CCITT: The International Telegraph and Telephone Consultative Committee.

CMOS: Complementary Metal Oxide Semiconductor — An implementation technology, (see page 110 and table 8.2).

DTDM: Dynamic TDM, (see page 11).

ECL: Emitter Coupled Logic — A high speed implementation technology, (see page 110 and table 8.2).

FDDI: Fiber Distributed Data Interface — A high speed local area network.

FIFO: First In First Out — A queueing discipline.

GaAs: Gallium Arsenide — A very high speed implementation technology, (see page 110 and table 8.2).

HCMOS: High speed CMOS — An implementation technology, (see page 99).

HDLC: High-level Data Link Control — A popular data link layer protocol.

I/O: Input/Output.

ISDN: Integrated Services Digital Network, (see page 5).

LAN: Local Area Network, (see page 3).

MAN: Metropolitan Area Network, (see page 4).

PABX: Private Automatic Branch Exchange — A private telephone exchange.

STM: Synchronous Transfer Mode, (see page 5).

TASI: Time Assignment Speech Interpolation, (see page 13).

TDM: Time Division Multiplexing, (see page 9).

TTL: Transistor Transistor Logic — An implementation technology.

VCI: Virtual Circuit Indicator, (see page 107).

VLSI: Very Large Scale Integration — An integrated circuit containing a large number of active devices.